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April 15, 2004

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JC715 U.S. PTO
60/459353
04/02/03

PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

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☑ *Additional inventors are being named on the* 1 *separately numbered sheet(s) attached hereto*

TITLE OF THE INVENTION (500 characters max)

MULTI-CHIP BALL GRID ARRAY PACKAGE AND METHOD OF MANUFACTURE

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23373

PATENT TRADEMARK OFFICE

ENCLOSED APPLICATION PARTS (*check all that apply*)

☑ Specification *Number of Pages* 6

☑ Drawing(s) *Number of Sheets* 4

☐ Application Data Sheet. See 37 CFR 1.76

☐ CD(s), Number

☐ Other (specify)

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT

☐ Applicant claims small entity status. See 37 CFR 1.27.

☑ A check or money order is enclosed to cover the Provisional filing fees. The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to **Deposit Account No. 19-4880.** Please also credit any overpayments to said Deposit Account.

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FILING FEE AMOUNT ($)

$160.00

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

☑ No.

☐ Yes, the name of the U.S. Government agency and the Government contract number are:

Respectfully submitted,

SIGNATURE

DATE April 2, 2003

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DOCKET NO. P74738

USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

PROVISIONAL APPLICATION FOR PATENT COVER SHEET
Additional Page

Docket Number	P74738

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This invention relates generally to the field of semiconductor IC (Integrated Circuit) packaging and more particularly to the field of multi-chip packaging. This invention discloses a novel method of multi-chip packaging that serves to overcome present difficulties of such that involves chips of similar or identical sizes and of non-periphery bond pad layout. Accordingly, this invention also provides for the design and process methodologies for the manufacture of this package.

In recent times, multi-chip packaging, which is a special field of IC packaging that relates to the assembly of multiple semiconductor chips within a single IC package entity, has become increasingly popular. This is mainly driven by industry demand to package more functional silicon content into smaller form factor packages at lower cost. Packaging two or more silicon IC within the same IC package body reduces the area required and related cost on the printed circuit boards, on which the IC packages are mounted. In addition, multi-chip packaging enables close proximity and shorter electronic signal path between the chips in the package. This reduces electronic signal travel time and improves overall speed and performance.

Generally in multi-chip packaging, the component chips can be stacked vertically or arranged side-by-side on the interposer within the package body. Figures 1 and 2 show examples of multi-chip packages in stacked and side-by-side arrangement respectively.

Interconnections between chips and the external terminals of the package can be achieved by conventional wire bonding, bumps in flip chip fashion, lead bonding or combinations of the abovementioned techniques. Stacking the chips vertically requires less package body area and hence smaller space on the printed circuit board compared to arranging them side-by-side. Chip stacking is generally the preferred method applied in multi-chip packaging. However, there are still presently several fundamental difficulties in chip stacking relating to stacking of chips of similar size and special bond pad layout designs.

a) For chips of similar sizes, they cannot be stacked directly on each other because the bonding pads on the bottom chip would be blocked when the next chip is stacked into them. This makes connections, for example by wire bonding, out of the chip to the external terminals of the package impossible.

b) For chips with non-periphery bond pad layout design, as shown in Figure 3, the probability of that the bond pads of the bottom chip being blocked is high even with smaller chip stacked on top. This also renders connection out of the bond pads of the bottom chip very difficult.

c) For chips with bond pads arranged in multiple rows in close proximity, as illustrated in Figure 3, it is necessary that the two chips to be facing the same direction in the package to maintain same orientation of the bond pads for after stacking to avoid complications in subsequent interconnect processes such as wire bonding.

The present invention provides a feasible solution for multiple chips of similar size and of non-periphery bond pad layout in a BGA package. Manufacturers could use this invention to increase the functional capacity, such as memory capacity of semiconductor memory IC chips, with significantly reduced need for package body area and printed circuit board space requirements. It is also possible that the secondary substrate structure, as shown in Figure 7B, be subject to testing. This would allow the functional status of the chip, whether it is good or bad, be known before attaching it to the base substrate. This would reduce the risk of combining a bad chip with a good one in multi-chip packaging (generally non-reversible process) and improves the final yield of the package.

The complete package structure, shown in Figure 11, comprises:

a. Semiconductor chips with bond pads for interconnection

b. Substrates that contain conductive patterned traces and vias to provide pathways for electrical signals between the semiconductor chips and the external terminals of the package.

c. Adhesive layers for attaching the semiconductor chip to the substrates.

d. Conductive fine wires that connect the bond pads on the semiconductor chips to the terminals pads on the substrates and also between the terminals of the substrates.

e. Encapsulant or molding compound that protects the semiconductor chips and related content with a defined body outline.

f. Solderballs that forms the external terminals of the package for connecting to the terminals on the printed circuit boards.

The present invention will now be described by way of non-limitative example only, with reference to the accompanying schematic drawings, in which:

Figures 3-11 show in perspective view successive steps in the method of packaging.

Figure 3A and 3B shows the 3D perspective of the base substrate and the secondary substrate respectively. An opening is present at the center of the substrate to allow subsequent interconnecting fine wires to pass through substrate in the later processes. There is an adhesive layer on each substrate for chip attachment onto the substrate.

Figure 4A shows the cross sectional view of the base substrate of the package structure. Conductive traces are present on the both surfaces of the substrate and they are protected by a layer of solder mask material which has had designated areas removed to reveal parts of the conductive traces for making subsequent interconnects. Vias are present to allow conductive traces to pass through to the opposite side of the substrate material. There is no restriction on the location of such vias on the base structure.

Figure 4B shows the cross sectional view of the secondary substrate of the package structure. This substrate has conductive traces on either side of the surface, an opening at the

center of the substrate, as well as adhesive layer for chip attachment. However, there is no solder mask layer and vias present in the secondary substrate.

Figures 5A and 5B show the structure of both the base and secondary substrate respectively after chip attachment. The chip surface of which the bond pads are present is adhered onto the adhesive layer on the substrate. The bond pads are left accessible through the opening of the substrates in each case.

Figures 6A and 6B show the connection between the bond pads and the terminal pads of the substrate structures by fine wires after the wire bonding process. Alternatively, the interconnect between the top chip and the secondary substrate can be established by tiny conductive bumps by a process called flip chip attach (see figure 6C).

Figure 7A shows the base substrate structure after a layer of adhesive had been applied onto the top surface of the chip. This layer serves as adhesive agent to attach the secondary substrate onto the base structure.

In the next step, shown in Figure 7B, the wire bonded side of the secondary substrate is encapsulated completely by a protective, inert material. This material protects the bottom surface of the secondary substrate and the wire connections within the opening of the substrate.

Figure 8 shows the package structure after the attachment of the secondary substrate onto the adhesive layer on the semiconductor chip of the base substrate structure. Typically, both substrate structures are aligned along their symmetrical axis.

In the next step, shown in Figure 9, fine wires are bonded to the terminals of the base and secondary substrate to establish electrical connection paths between the two structures.

In Figure 10, the entire package structure and the wire bond at the opening of the base substrate is encapsulated by molding compound. The molding compound serves as protective housing for the package.

Figure 11 shows the attachment of conductive solderballs to the bottom of the package. The conductive solderballs serves as connecting terminals to the printed circuit boards on which the package would be mounted.

Other possible derivation of the package configurations are described as follows:

a) It is possible that the silicon surface of the top chip be left exposed (see Figure 12). This allows for the overall package height to be reduced in applications that has space constraints, such as mobile handsets and personal digital assistant (PDAs).

b) It is possible for additional secondary structure to be stacked on top of each other as shown in figure 13.

c) It is possible to add in thermal enhancement features, such a thermal conductive heat sink on top of the secondary structure to improve the thermal dissipation capability of the package. (see Figure 14)

CLAIMS

1. A semiconductor package comprising:

semiconductor chips with bond pads for interconnection,

substrates that contain conductive patterned traces and vias to provide pathways for electrical signals between the semiconductor chips and the external terminals of the package,

adhesive layers for attaching the semiconductor chip to the substrates,

conductive fine wires that connect the bond pads on the semiconductor chips to the terminals pads on the substrates and also between the terminals of the substrates,

encapsulant or molding compound that protects the semiconductor chips and related content with a defined body outline,

solderballs to act as external terminals of the package for connecting to the terminals on the printed circuit boards.

2. A semiconductor package comprising any part of the structure described in Claim 1. This includes additional features of exposed silicon (as shown in Figure 12), stack up of additional secondary structure (see figure 13) and heat sink (see Figure 14).

3. A semiconductor package comprising the structure and material according to Figure 7B of the accompanying drawings.

4. A substrate structure comprising exposed electrically conductive traces on either side of the surface and an opening in the substrate as illustrated in Figure 4B.

5. A method of packaging semiconductor chips in accordance to the constructional sequence as described with reference to Figures 4 to 11 the accompanying drawings.

Illustrations (1/4)

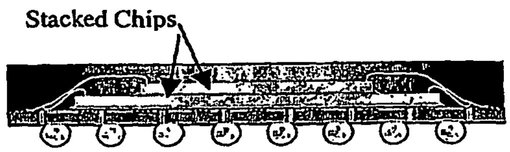

Figure 1A

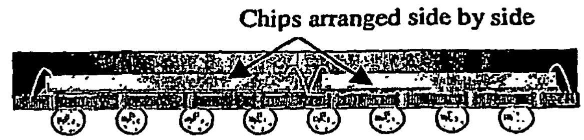

Figure 1B

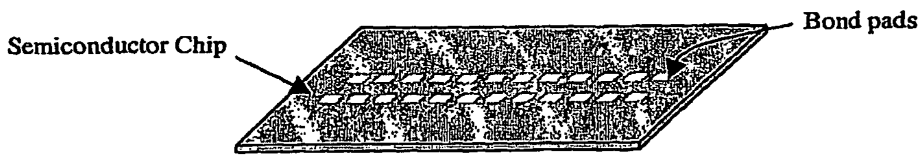

Figure 2

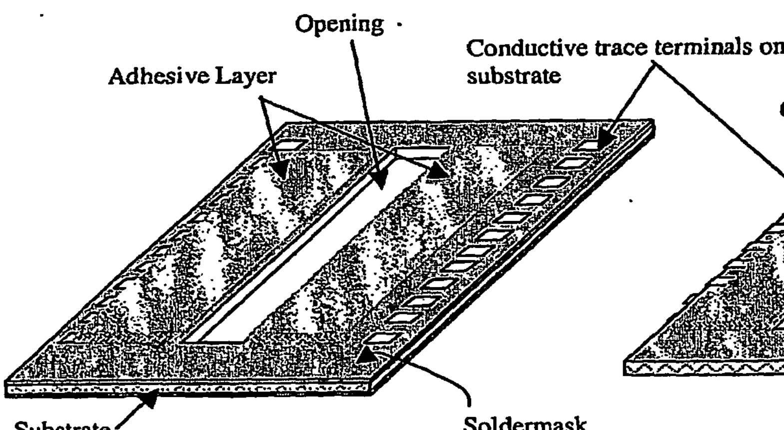

Figure 3A

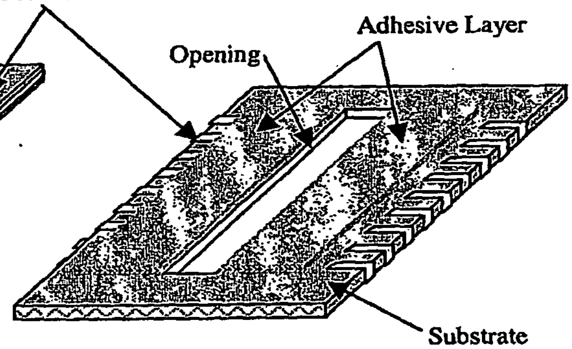

Figure 3B

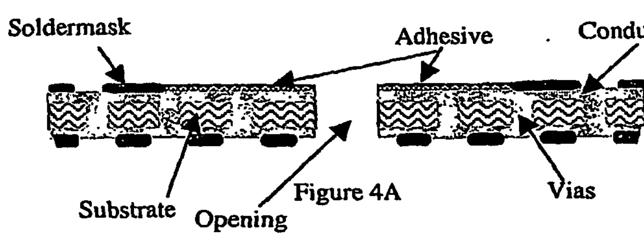

Figure 4A

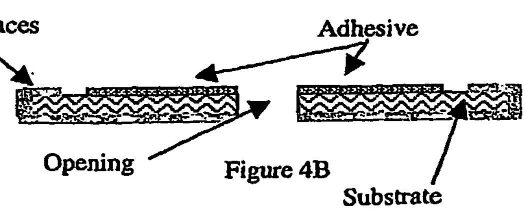

Figure 4B

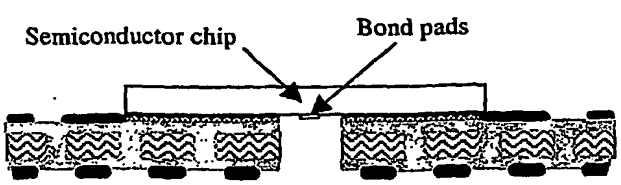

Figure 5A

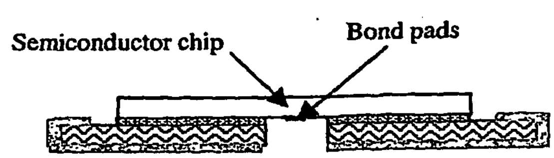

Figure 5B

Illustrations (2/4)

Figure 6A

Figure 6B

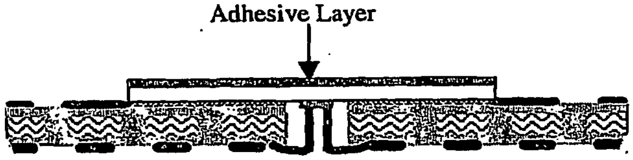

Figure 7A

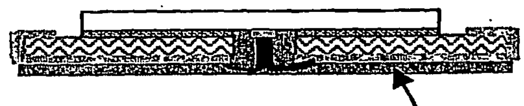

Figure 7B

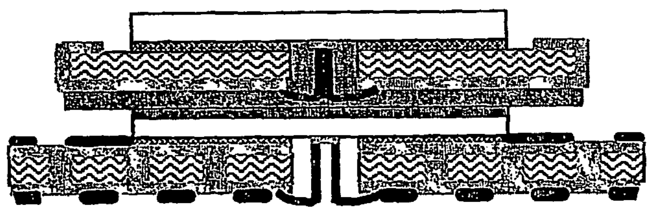

Figure 8

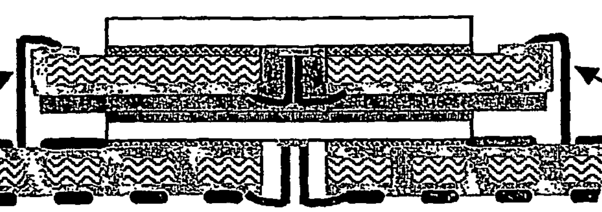

Figure 9

Illustrations (3/4)

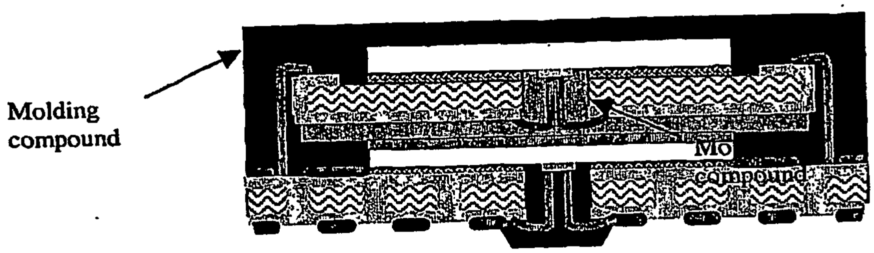

Figure 10

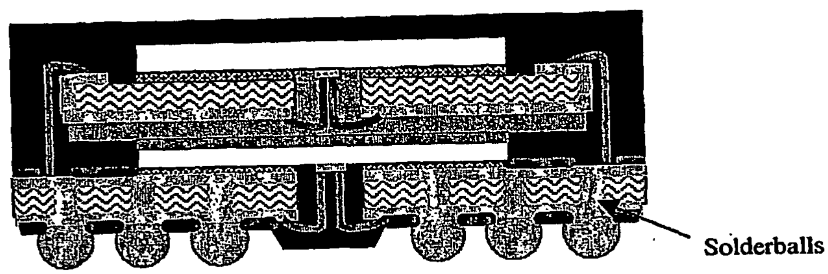

Figure 11

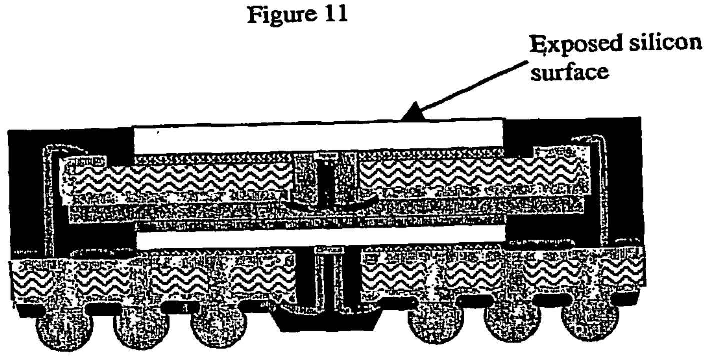

Figure 12

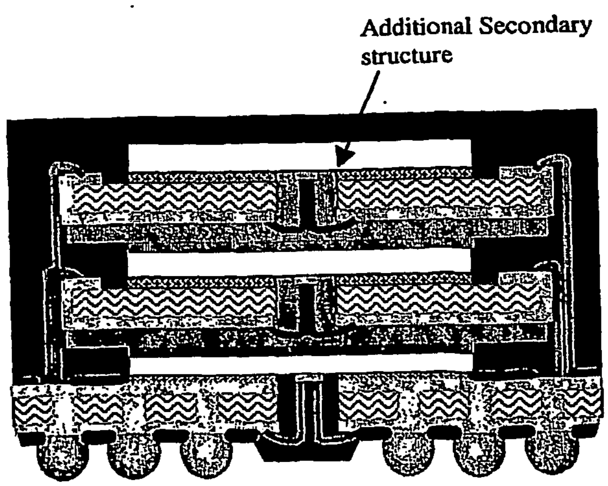

Figure 13

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Illustrations (4/4)

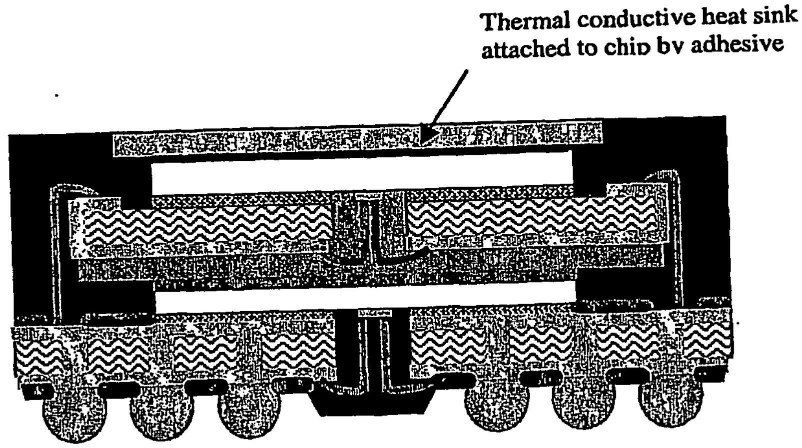

Figure 14